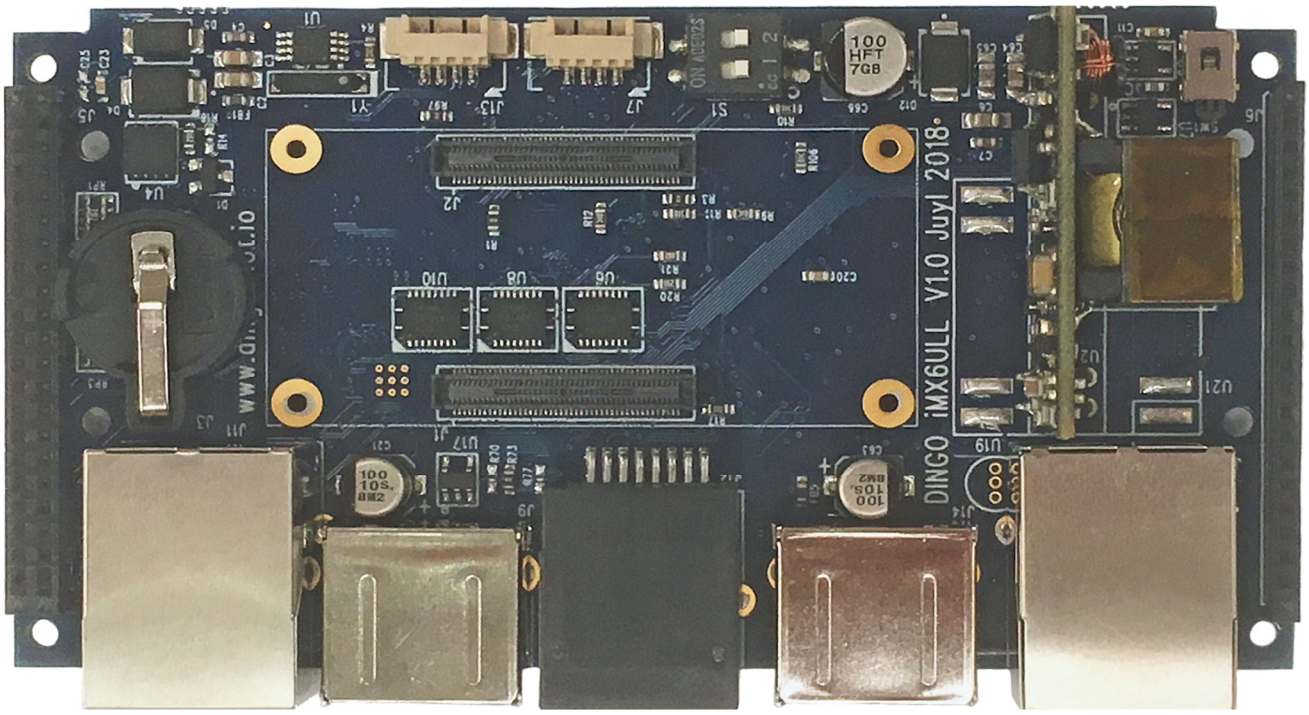
DINGO BACKBONE

DINGO NXP iMX6ULL Compute Board

DATASHEET COMPLETE

Item specifications

Go-IoT Item Id:	OPTION	DINGO-CB-IMX6ULL
CPU		Freescale i.MX6UltraLite/6ULL
	1	533MHz
	2	800MHz – Industrial Range
	3	900MHz – Commercial Range
RAM	A	LvDDR3 128MByte
	B	LvDDR3 512MByte
NAND	C	512MByte
eMMC	D	8GByte
SD Holder		Upto 64GByte uSD Card
Ethernet		2 x 10/100 Mbps with Link / Activity LEDs
Ethernet POE	E	802.11af POE – 12.95W
WiFi	F	Certified 802.11 b.g.n.ac
Bluetooth	G	4.2 + BLE
Secure Authentication	H	NXP A7101
USB		1 x USB 2.0 Type A Connector 4 x USB 2.0 Ports to Base Board
Serial Interface		1 x RS232 via RJ45 Connector 1 x RS485 via RJ45 Connector 1 x TTL Serial Debug Connector 4 x TTL Serial Ports to Base Board
HDMI Video Output		None
1-Wire Interface		1 x 1-Wire Interface via RJ45 Connector
Real Time Clock		ISL12057 with Battery Backup
EEPROM		24LC32 – 4K x 8
I2C Ports		4
SPI Ports		1
Expansion Connectors		1 x 40way header to Base Board 1 x 20way header to Base Board 1 x 30way header to Display Board 21 x GPIO
OS		Linux Debian Stretch Yocto Krogoth/Morty/Pyro/Rocko Boot2QT Morty
DC Input		+12V @ 0.6A
Size (L x W x H)		101 x 60 x 19 mm
Temperature		-20degree C to +85degree C
Country of Manufacture:		EU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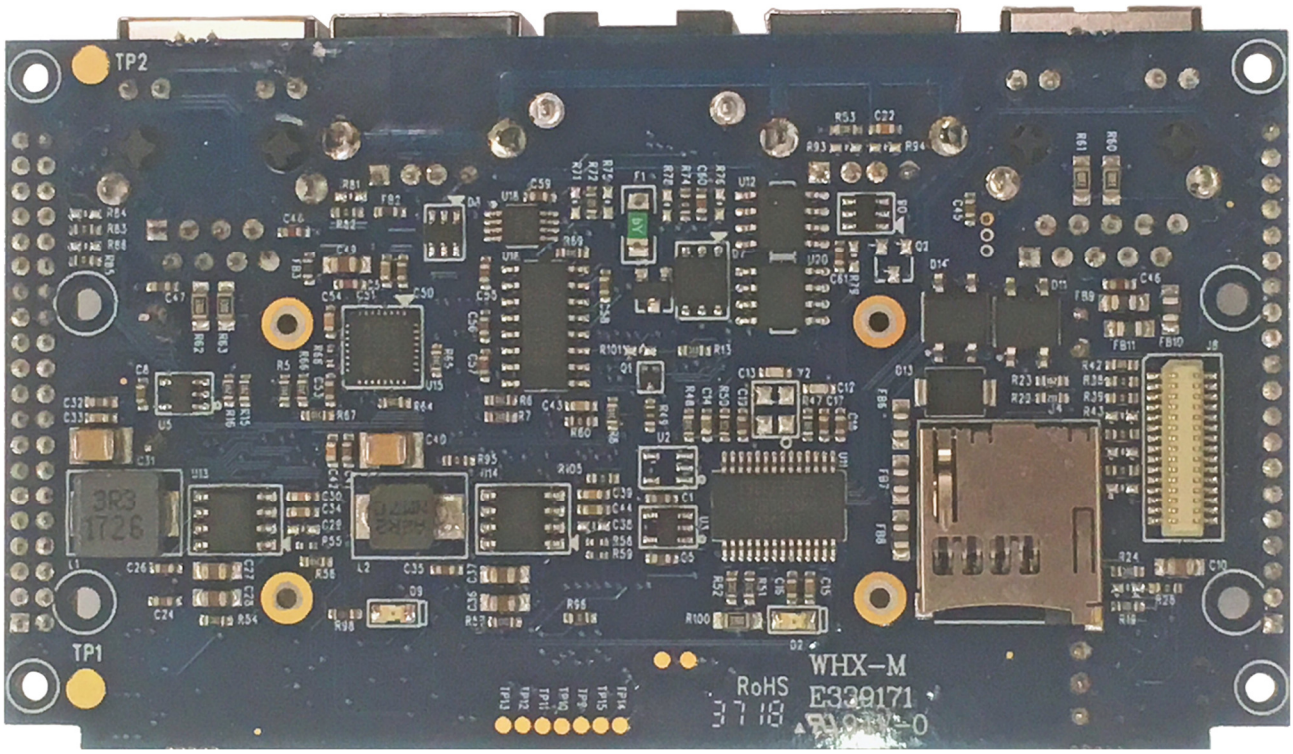

TP2
TP1
WHX-M
RoHS
E339171

CPU Module

The DART-6UL/DART-6UL-5G is a power-optimized cost-effective System-on-Module that perfectly fits various embedded and industrial products and segment. It is based on i.MX6 Ultralight/ 6ULL up to 900MHz ARM® Cortex™-A7 multipurpose processor from NXP/Freescale. The DART-6UL/DART-6UL-5Gprovides an ideal building block for simple integration with a wide range of products in target markets requiring low power consumption, small size and a very cost-effective solution.

CPU Platform

The i.MX 6UltraLite / 6ULL processors are based on ARM Cortex-A7 MPCore™ Platform, which has the following features: • Supports single ARM Cortex-A7 MPCore (with TrustZone) with: ✓ 32 KByte L1 Instruction Cache ✓ 32 KByte L1 Data Cache ✓ Private Timer and Watchdog ✓ Cortex-A7 NEON MPE (Media Processing Engine) Co-processor • General Interrupt Controller (GIC) with 128 interrupts support • Global Timer • Snoop Control Unit (SCU) • 128 KB unified I/D L2 cache • Single Master AXI bus interface output of L2 cache • NEON MPE coprocessor ✓ SIMD Media Processing Architecture ✓ NEON register file with 32x64-bit general-purpose registers ✓ NEON Integer execute pipeline (ALU, Shift, MAC) ✓ NEON dual, single-precision floating point execute pipeline (FADD, FMUL) ✓ NEON load/store and permute pipeline ✓ 32 double-precision VFPv3 floating point registers.

Memory Interfaces

The SoC-level memory system consists of the following additional components: • Boot ROM, including HAB (96 KB) • Internal multimedia/shared, fast access RAM (OCRAM, 128 KB) • Secure/non-secure RAM (32 KB) External memory interfaces: The i.MX 6UltraLite / 6ULL processors support latest, high volume, cost effective handheld DRAM, NOR, and NAND Flash memory standards. SoM Supports: • 16-bit LV-DDR3-800 • 8-bit NAND-Flash

RAM

The DART-6UL/DART-6UL-5G is available with up to 512MB of DDR3L memory.

Non-volatile Storage Memory

The DART-6UL/DART-6UL-5G is available with a variety of non-volatile storage memory options, used for Flash Disk purposes, O.S. run-time-image, Boot-loader and application/user data storage.

The DART-6UL/DART-6UL-5G can arrive with up to 512MB SLC NAND flash or up to 32GB MLC eMMC (note: it is not possible to use both on-SOM NAND and eMMC at the same time).

uSD Card Interface

J4 Provides a uSD Interface. The uSD Card interface is driven by the SD1 interface of the of the DART-6UL. This interface used by on SoM Wi-Fi module, so it is accessible only when the Wi-Fi module is disabled. This connector mainly used for development and program update of the SoM internal storage.

USB Hub

The iMX6ULL has two USB Ports – The first USB Port is connected to the USB HUB while the second USB port is connected to a Genesys GL852 4 Port Hub that provides USB Connectivity to the USB Ports on the Base Board

10/100 Ethernet Controller

The core implements a dual speed 10/100 Mbit/s Ethernet MAC compliant with the IEEE802.3-2002 standard. The MAC layer provides compatibility with half- or full duplex 10/100 Mbit/s Ethernet LANs. The MAC operation is fully programmable and can be used in Network Interface Card (NIC), bridging, or switching applications. The core implements the remote network monitoring (RMON) counters according to IETF RFC 2819. The core also implements a hardware acceleration block to optimize the performance of network controllers providing TCP/IP, UDP, and ICMP protocol services. The acceleration block performs critical functions in hardware, which are typically implemented with large software overhead.

10/100 Ethernet PHY

The iMX6ULL features Micrel™ KSZ8081RNL Ethernet PHY's. KSZ8081 is a single supply 10Base-T/100BaseTX Ethernet physical-layer transceiver for transmission and reception of data over standard CAT-5 unshielded twisted pair (UTP) cable. The KSZ8081 is a highly integrated PHY solution. It reduces the board cost and simplifies board layout by using on-chip termination resistors for the differential pairs and by integrating a low noise regulator to supply the 1.2V core and by offering 1.8/2.5/3.3V

Power Over Ethernet (PoE)

An IEEE802.11AF PoE Module is connected to J10 Magjack providing an alternative method of Powering the iMX6ULL and DINgo.

Wi-Fi + BT 2.5.1. DART-6UL-5G

The DART-6UL-5G contains LSR's pre-certified high-performance Sterling-LWB5™ Dual band 2.4/5 GHz Wi-Fi® and Bluetooth® Smart Ready Multi-Standard Module based upon the Cypress (formerly Broadcom) CYW43353 chipset supporting 802.11 ac/a/b/g/n, BT 2.1+EDR, and BLE 4.2 wireless connectivity. 2.5.2. The DART-6UL contains LSR's pre-certified high-performance Sterling-LWB™ 2.4 GHz Wi-Fi® and Bluetooth® Smart Ready Multi-Standard Module based upon the Cypress (formerly Broadcom) CYW4343W chipset supporting IEEE 802.11 b/g/n, BT 2.1+EDR, and BLE 4.2 wireless connectivity.

Both the DART-6UL/DART-6UL-5G modules realize the necessary PHY/MAC layers to support WLAN applications in conjunction with a host processor over a SDIO interface. The modules also provide a Bluetooth/BLE platform through the HCI transport layer. Both WLAN and Bluetooth share the same antenna port.

DART-6UL/DART-6UL-5G Key Features:

- IEEE 802.11 ac/a/b/g/n (DART-6UL-5G)
- IEEE 802.11 b/g/n (DART-6UL)
- Bluetooth 2.1+EDR, and BLE 4.2
- U.FL connector for external antenna
- Latest Linux and Android drivers supported directly by LSR and Cypress

• SIG certified Bluetooth driver • Wi-Fi/BT module Broad certifications with multiple antennas: FCC (USA), IC (Canada), ETSI (Europe), Giteki (Japan), and RCM (AU/NZ)

• Industrial operating Temperature Range: -40 to +85

Serial Interfaces

The iMX6ULL exposes 6 UART Serial Interfaces on the external connectors and internal devices

I2C is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices.

ON Board Serial Interfaces

Serial I/F	Connector	Description	Location
ttycx0	J7	Console Debug	IMX6ULL
ttycx1	None	Blue Tooth	DART Module
Ttycx2	J12	RS485	IMX6ULL
ttycx4	J12	RS232	IMX6ULL

OFF Board Serial Interfaces

Serial I/F	Connector	Description	Location
ttycx2	J5	Serial UART	Baseboard
ttycx5	J5	Serial UART	Baseboard

Boot Select (SW1)

The Boot select switches SW1 sets the iMX6ULL boot source & sequence.

SW1-1	SW1-2	Boot Source
OFF	OFF	SD Card
OFF	ON	eMMC
ON	OFF	NAND
ON	ON	NAND

SPI Interface

The iMX6ULL exposes 1 ISPI interfaces on the external connectors J5 and J8.

RTC

There is an ISL12057 Real Time Clock along with Battery Back on the PCB.

This in under Linux Kernel Control.

I2C Interface

The iMX6ULL exposes 4 I2C interfaces on the external connectors and internal I2C Interfaces.

I2C is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices.

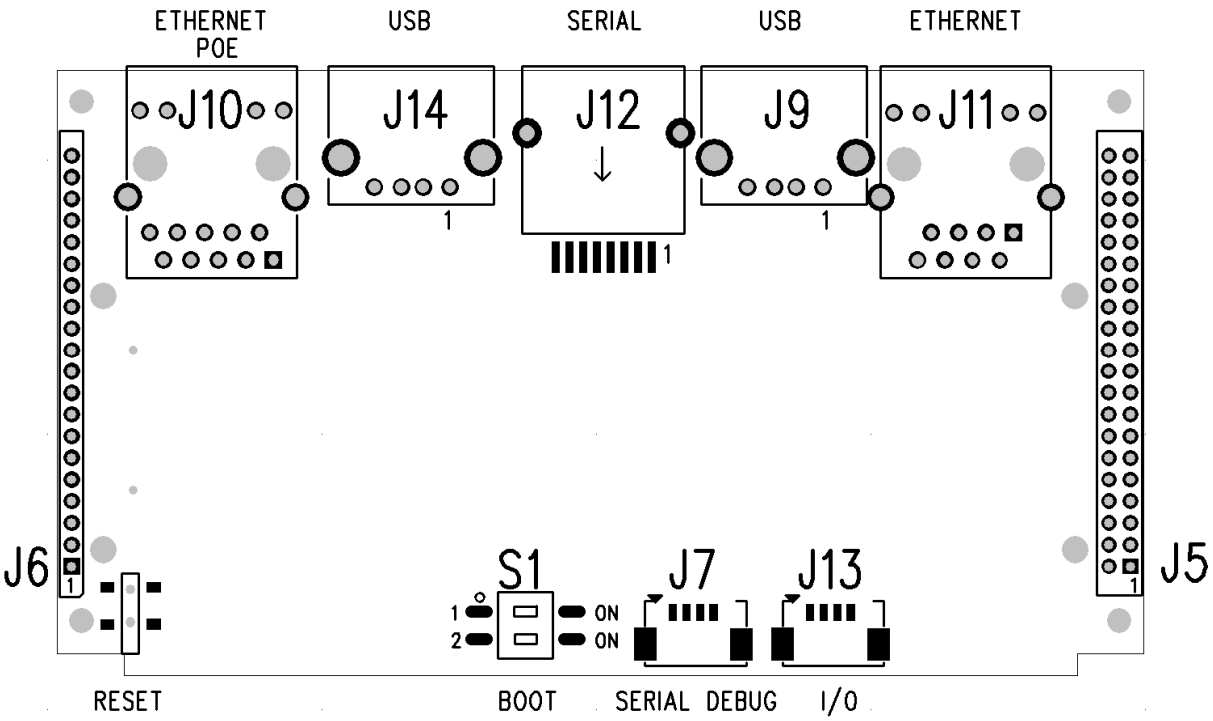
ON Board I2C Devices

Ch No	Device	Address	Description	Location
0	DS2482	0x18	I1Wire	IMX6ULL
0	A7101CHTK2	0x48	Security	IMX6ULL
0	AT24C32	0x50	EEPROM	IMX6ULL
1	Audio Codec	0x18	??	DART
1	EEPROM	0x50	??	DART
1	EEPROM	0x51	??	DART
1	ISL12057	0x68	RTC	IMX6ULL

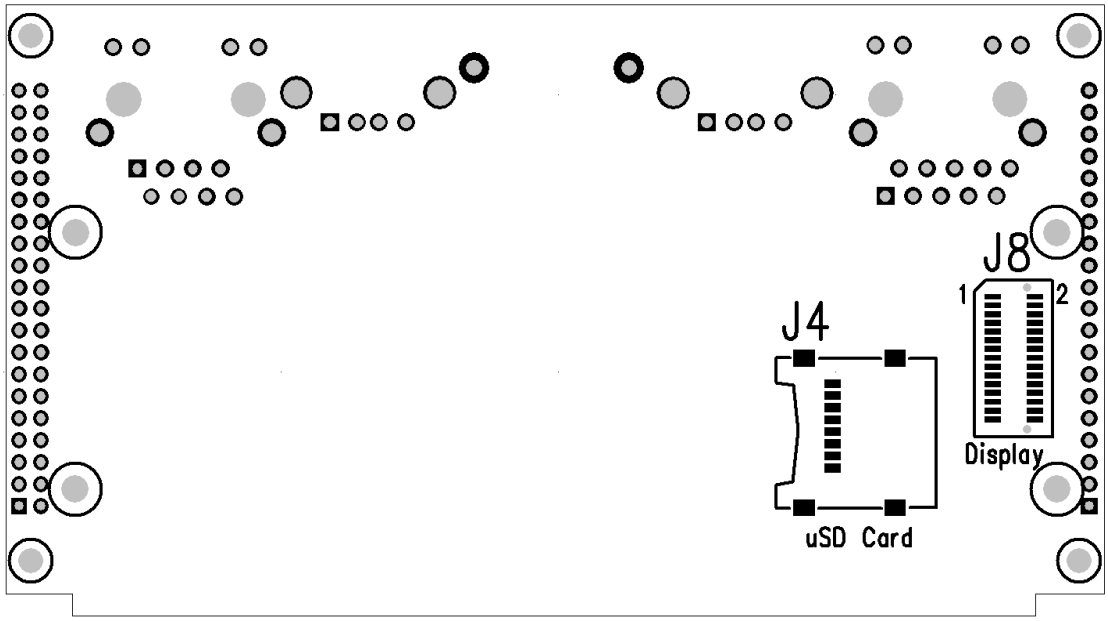
OFF Board I2C Devices

Ch No	Device	Address	Description	Location
0/2	TLC59116	0x60	LED Driver1	LED PCB
0/2	TLC59116	0x61	LED Driver 2	LED PCB
0/2	TLC59116 All Call Address	0xd0	LED Driver 1/2	LED PCB
0/2	128 x 64 LCD	0x3C	LCD 128x64	LED PCB
0	PCF8574A	0x3e	I/O Expander	LCD PCB Keys/LEDs
0	PCF8574A	0x3f	I/O Expander	Baseboard - FETs
1	PCF8574A	0x40	I/O Expander	Plug In Position 1(RHS)
1	PCF8574A	0x41	I/O Expander	Plug In Position 2
1	PCF8574A	0x42	I/O Expander	Plug In Position 3
1	PCF8574A	0x43	I/O Expander	Plug In Position 4(LHS)
1	PCF8574A	0x44	I/O Expander	SimpleLink Plug In (temp)
1	PCF8574A	0x45	I/O Expander	Xbee Plug In (temp)
1	24LC32	0x54	EEPROM	Plug In Position 1(RHS)
1	24LC32	0x55	EEPROM	Plug In Position 2
1	24LC32	0x56	EEPROM	Plug In Position 3
1	24LC32	0x57	EEPROM	Plug In Position 4(LHS)
1	MCP3424-E/SL	0x6e	ADC	ADC Plug In

Top Side Connectors



Bottom Side Connectors



J5 – 40WAY GPIO TO BASEBOARD

Pin	Port	Dir	Pull Up	Function	Description
1	+12V	IN		POWER	Main Power IN +12V DC
2	+12V	IN		POWER	Main Power IN +12V DC
3	GPIO3_23	OUT	NO	RELAY 1	Logic 1 – Activate Relay 1
4	GPIO1_0	IN	YES	OPTO	Opto Input 1
5	GPIO3_24	OUT	NO	RELAY 1	Logic 1 – Activate Relay 2
6	GPIO1_1	IN	YES	OPTO	Opto Input 2
7	SPI_CLK	OUT	NO	SPI	GPIO11 – SPI Clock
8	GPIO1_2	IN	YES	OPTO	Opto Input 3
9	SPI_MOSI	OUT	NO	SPI	GPIO10 - SPI Master Out – Slave In
10	GPIO1_4	IN	YES	OPTO	Opto Input 4
11	SPI_MISO	IN	NO	SPI	GPIO9 - SPI Master In – Slave Out
12	GPIO1_5	IN	YES	OPTO	Opto Input 5
13	SPI_SS0	OUT	NO	SPI	GPIO8 - SPI Slave Select 0 – Plug In 3
14	GPIO1_9	IN	YES	OPTO	Opto Input 6
15	SPI_SS1	OUT	NO	SPI	GPIO7 - SPI Slave Select 1 – Plug In 2
16	GPIO5_1	IN	YES	OPTO	Opto Input 7
17	SPI_SS2	OUT	NO	SPI	GPIO34 - SPI Slave Select 2 – Plug In 1
18	GPIO5_5	IN	YES	OPTO	Opto Input 8
19	GPIO4_21	IN	YES	EVENT	EVENT from N-PLC - Plug In 1
20	GPIO4_22	IN	YES	EVENT	EVENT from N-PLC - Plug In 2
21	GPIO4_23	IN	YES	EVENT	EVENT from N-PLC - Plug In 3
22	GPIO4_24	IN	YES	EVENT	EVENT from N-PLC - Plug In 4
23	TXD7	OUT	YES	UART	TXD to N-PLC All Plug Ins
24	RXD7	IN	YES	UART	RXD from N-PLC All Plug Ins
25	+5V	OUT		POWER	+5V Output – 2A available
26	+5V	OUT		POWER	+5V Output – 2A available
27	GND			POWER	GROUND
28	GND			POWER	GROUND
29	USB DN			USB	USB Channel 1 D- to Base Board Plug In 1
30	USB DP			USB	USB Channel 1 D+ to Base Board Plug In 1
31	RTC Battery			POWER	Larger RTC Backup if required
32	NC				spare
33	I2C1_SCL	OUT	YES	I2C	I2C Channel 1 Clock
34	I2C1_SDA	BI	YES	I2C	I2C Channel 1 Data
35	GPIO5_8	bi	NO		Spare
36	CTS3	IN	YES	UART	CTS from Baseboard – All Plug Ins
37	TXD3	OUT	NO	UART	TXD to Baseboard – All Plug Ins
38	RXD3	IN	YES	UART	RXD from Baseboard – All Plug Ins
39	RTS3	OUT	NO	UART	RTS to Baseboard – All Plug Ins
40	GND			POWER	GROUND

J6 – 20WAY GPIO TO BASEBOARD

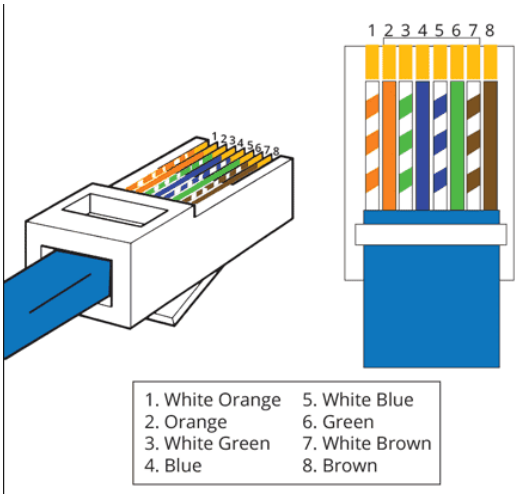
Pin	Port	Dir	Pull Up	Function	Description
1	+3.3V	OUT		POWER	+3.3V Output – 300mA available
2	I2C_SDA1	BI	YES	I2C	I2C Channel 1 Data
3	GND			POWER	GROUND
4	GND			POWER	GROUND
5	RTS3	OUT	NO	UART	RXD from Baseboard – All Plug Ins
6	GPIO3_13	OUT	NO	BOOT	BOOT to N-PLC Station 2
7	I2C_SCL1	OUT	YES	I2C	I2C Channel 0 Clock
8	TXD_CON	OUT	NO	UART	TXD – Debug Console
9	RXD_CON	IN	YES	UART	RXD – Debug Console
10	GPIO3_14	OUT	NO	BOOT	BOOT to N-PLC Station 1
11	GPIO3_15	OUT	NO	BOOT	BOOT to N-PLC Station 3
12	USB DP			USB	USB Channel 4 D+ to Base Board 4
13	GPIO3_16			GPIO	Battery ON -1 = Battery Backup
14	USB DN			USB	USB Channel 4 D- to Base Board 4
15	+5V	OUT		POWER	+5V Output – 2A available
16	USB DP	BI	NO	USB	USB Channel 3 D+ to Base Board 2
17	USB DN	BI	NO	USB	USB Channel 3 D- to Base Board 2
18	USB DP	BI	NO	USB	USB Channel 4 D+ to Base Board 3
19	USB DN	BI	NO	USB	USB Channel 4 D- to Base Board 3
20	GND			POWER	GROUND

J7 – 4WAY Console debug

Pin	Port	Dir	Function	Description
1	+3.3V		POWER	+3.3V Output – 300mA available
2	TX Data	OUT	UART	TTL TXD
3	RX Data	IN	UART	TTL RXD
4	GND		POWER	GROUND

J12 – 8WAY RJ45 – PCB Version 2.2 – July 2018 onwards

Pin	Port	Dir	Function	Description
1	TXD RS232	OUT	UART	RS232 – TXD 1 WIRE +5V – 100mA Fuse
2	RXD RS232	IN	UART	RS232 – RXD
3	TX-/RX- RS485	BI	UART	RS485 –TX/RX- MODBUS "**A**" Half Duplex – 120OHM Termination Resistor (see below)
4	1 WIRE VCC	OUT	POWER	1 WIRE +5V – 100mA Fuse
5	GND		POWER	GROUND
6	TX+/RX+ RS485	BI	UART	RS485 –TX/RX- MODBUS "**B**" Half Duplex – 120OHM Termination Resistor (see below)
7	1 WIRE DATA	BI	1 WIRE	1 WIRE DATA
8	1 WIRE GND		1 WIRE	1 WIRE GROUND



An RS-485 bus consists of multiple transceivers connected in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, allows for relatively high data rates over long cable lengths.

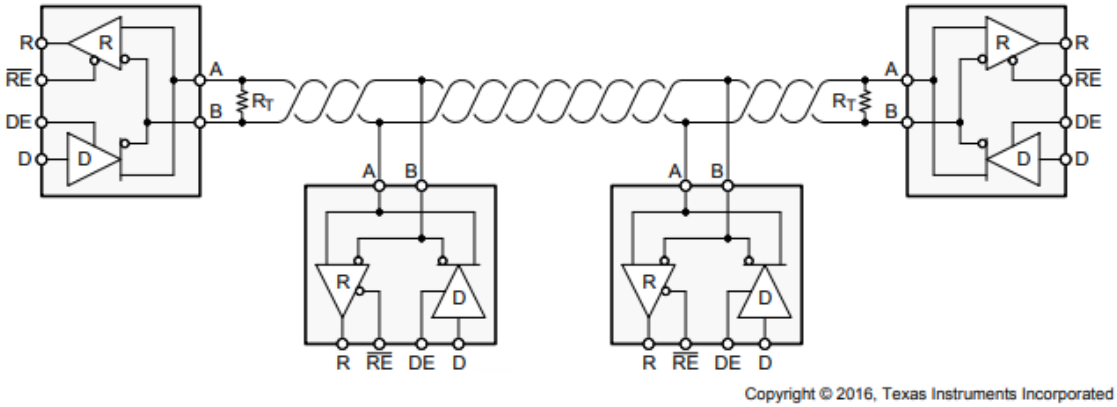


Figure 20. Typical RS-485 Network With SN65HVD7x Transceivers

Note: The A & B above are NOT the MODBUS Convention

GO-IOT labels the data lines on RS-422 and RS-485 with an "A", for negative or "B" for positive (at the connector), to indicate the positive and negative relationship between the two data lines. It is important to label the data lines because this positive and negative relationship between the lines must be maintained when connecting one device to another.

Reversing the two lines in the differential signal is by far the most common initial error when connecting two pieces of RS-422 or RS-485 equipment. The good news is that it won't cause any damage to your equipment to try it the wrong way. If you try it connected one way and are seeing garbled data, reverse the leads and try again. If this doesn't instill a level of confidence you are comfortable with, or you have tried both combinations with negative results, you can usually use a DC voltmeter to determine which line is which. 1. Measure the voltage across the two lines at the receiver without the driver connected. On an RS-485 device the driver and receiver are on the same pair. 2. Note which signal line the positive lead of the voltmeter is connected to. 3. Is the reading positive or negative? 4. If the reading is positive, the signal line going to the positive lead of the voltmeter corresponds to the "B" line of the RS-422/485 standards. 5. If the reading is negative, the signal line going to the positive lead of the voltmeter corresponds to the "A" line of the RS-422/485 standards.

J8 – 30WAY GPIO TO LED / LCD DISPLAY PCB

Pin	Port	Dir	Pull Up	Function	Description
1	+5V	OUT		POWER	+5V Output – 1A available
2	+5V	OUT		POWER	+5V Output – 1A available
3	+5V	OUT		POWER	+5V Output – 1A available
4	+5V	OUT		POWER	+5V Output – 1A available
5	I2C_SCL1	OUT	YES	I2C0	I2C – Channel 1 Clock
6	SPI_MISO	IN		SPI	SPI Master In – Slave Out – LCD I/F
7	I2C_SDA1	BI DI	YES	I2C0	I2C – Channel 1 Data
8	SPI_MOSI	OUT		SPI	SPI Master Out – Slave In – LCD I/F
9	I2C_SCL	OUT	YES	I2C1	I2C – Channel 1 Clock
10	SPI_CLK	OUT		SPI	SPI Clock – LCD I/F
11	I2C_SDA	IN	YES	I2C1	I2C – Channel 1 Data
12	SPI_SS0	OUT		SPI	SPI Slave Select 0 – LCD I/F
13	SPI_SS2	OUT		SPI	SPI Slave Select 2
14	SPI_SS1	OUT		SPI	SPI Slave Select 1
15	+3.3V	OUT		POWER	+3.3V Output – 300mA available
16	+3.3V	OUT		POWER	+3.3V Output – 300mA available
17	+3.3V	OUT		POWER	+3.3V Output – 300mA available
18	+3.3V	OUT		POWER	+3.3V Output – 300mA available
19	GPIO3_17	IN		INT	I2C INTERRUPT – I2C Switches
20	GPIO3_20				Spare
21	GPIO3_18	OUT		GPIO	LCD BACKLIGHT ON/OFF - PWM
22	SPI_SS2	OUT		SPI	SPI Slave Select 3
23	GPIO3_19	OUT		GPIO	SPI DATA/CMD for LCD
24	nPOR	OUT		RESET	RESET – Active Low
25	+12V	OUT		POWER	+12V DC OUT
26	+12V	OUT		POWER	+12V DC OUT
27	GND			POWER	GROUND
28	GND			POWER	GROUND
29	GND			POWER	GROUND
30	GND			POWER	GROUND

J13 – 4WAY Expansion

Pin	Port	Dir	Function	Description
1	GPIO3_24		Spare	Spare
2	GPIO3_23		Spare	Spare
3	GPIO3_09		Spare	Spare
4	GPIO3_04		Spare	Spare

Programming Debian onto iMX6UL Module

7 Linux console access

User name	User password	User descriptor
root	root	system administrator
user	user	local user
x_user		used for X session access

8 Flash images to NAND flash / eMMC

In case you are using a SOM with NAND flash, run the following command **as root** to install Debian on it:

```
# debian-nand.sh
```

In case you are using a SOM with eMMC, run the following command **as root** to install Debian on it:

```
# debian-emmc.sh
```

The above scripts are located in /usr/sbin in the rootfs of the SD card used to boot Debian.

9 How-to: Test and use an interface

Please see this section in the Yocto developer guide page. It is the same for Debian.

10 How-to: Modify the kernel configuration

To modify the kernel configuration (add/remove features and drivers) please follow the steps below:

```
1. $ cd ~/var_mx6ul_dart_debian/src/kernel
2. $ sudo make ARCH=arm mrproper
3. $ sudo make ARCH=arm imx_v7_var_defconfig
4. $ sudo make ARCH=arm menuconfig
5. Navigate the menu and select the desired kernel functionality
6. Exit the menu and answer "Yes" when asked "Do you wish to save your new configuration?"
7. $ sudo make ARCH=arm savedefconfig
8. $ sudo cp arch/arm/configs/imx_v7_var_defconfig arch/arm/configs/imx_v7_var_defconfig.orig
9. $ sudo cp defconfig arch/arm/configs/imx_v7_var_defconfig
10. Follow the instructions above to rebuild kernel and modules, repack rootfs images and recreate SD card
```

Building Debian Image

http://variwiki.com/index.php?title=Debian_Build_Release&release=RELEASE_STRETCH_V1.0_DART-6ULroot